#16

[TITLE OF THE INVENTION]

ELECTRO-OPTICAL DEVICE

BACKGROUND OF THE INVENTION

[()Field of the Invention[)]

This invention relates to an electro-optical device and more particularly, to an active-type liquid crystal display device in which clear gradated display levels can be set.

[()Description of the Prior Art[)]

Because of the physical characteristics of the liquid crystal composition, the dielectric constant [thereof] of such compositions differs between a direction parallel to the molecule axis and a direction perpendicular to the molecule axis [, which]. This phenomena is referred to as dielectric anisotropy[, therefore]. Thus, the liquid crystals in the composition can easily be arranged parallel to or perpendicular to an external electric field. A liquid crystal electro-optical device utilizes this dielectric anisotropy, so that the ON/OFF display [is] characteristics are achieved by controlling the amount of light transmitted or the amount of light dispersion.

The electro-optical characteristics of a nematic liquid crystal are shown in FIG. 2. The relationship between the applied voltage and the transmissivity (amount of light transmitted) is as follows[;]:

	the applied voltage	the light transmitted
smaller	Va at point A 201	0%;
	Vb at point B 202	about 30%;

Vc at point C 203 about 80%;

larger Vd at point D 204 about 100%.

In short, if only points A and D are utilized, the two gradations, black and white, are displayed, and if the rising portion of the electro-optical characteristic curve is utilized, such as at points B and C, an intermediate gradated display is possible. [

]It [was] has been confirmed that Va=2.0V, Vb=2.18V, Vc=2.3V and Vd=2.5V.

Conventionally, in the case of a liquid crystal electro-optical device with a gradated display utilizing a TFT, the applied gate voltage or voltage applied over the source and drains of the TFT is varied to adjust the voltage, so that an [analogue] analog gradated display is obtained.

The gradated display method with a liquid crystal electro-optical device utilizing TFTs is further described below in detail.

An n-channel thin film transistor conventionally utilized in a liquid crystal electro-optical device has the voltage-current characteristic as shown in Fig.20. In the drawing, numeral 301 designates the characteristic in case of an n-channel thin film transistor using amorphous silicon, while numeral 302 designates the characteristic in case of an n-channel thin film transistor using polycrystalline silicon.

In a conventional gradated display method, by controlling analog voltages to be applied to the gate electrode, drain currents can be controlled, and accordingly, the resistance value between the source and the drain can be changed. As a result, the strength of the electric fields to be applied to the liquid crystal, connected [thereto] in series thereto, can be

arbitrarily changed by the division of the resistance, whereby a gradated display is made possible.

Also there is another conventional method, where the gate electrode is connected to scanning signal lines and the voltage between the source and drain is changed, resulting in controlling arbitrarily the electric field value itself to be applied to the liquid crystal.

Both of the above methods are [analogue] analog gradated display methods, largely relying upon the TFT characteristics. It is however difficult to form numbers of TFTs for matrix composition so as to make all of them have [an] a uniform electric characteristic. Particularly, it is extremely difficult , in the present circumstances, to finely adjust the intermediate voltage necessary for a gradated display by the present techniques. As can be realized by the electro-optical characteristics of a nematic liquid crystal shown in Fig.2, a gradated display has to be carried out within 0.32V[, that is] (i.e., from around 2.08V, the boundary value of dark condition, to around 2.40V, the boundary value of light condition). In the case of a gradated display of 16 gradations, the control of the voltage at every 0.02V in average is required.

On the other hand, when the voltage is controlled at such as point A 201 and point D 204 shown in Fig.2 where liquid crystal is completely turned ON/OFF, the difference between voltages of 0.5V or more can be obtained[, which]. The difference will sufficiently ease the variation in TFT characteristics. When, using a plurality of write-in frames, for example 6 frames among 10 frames are turned ON (at 2.5V) and the remaining 4 frames are turned OFF (2.0V), the write-in voltage is 2.3V in average, so that an intermediate gradated display becomes possible.

In this case, however, the drive frequency might be decreased

to 30Hz or lower which is not discernible by the human eyes. Depending on conditions, this becomes a cause of [the inferiority of] flicker in a display [such as flicker]. Although it is proposed to raise the drive frequency to prevent the above problem, the data transfer speed of a driver IC has its limit up to about 20MHz.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a means of supplying a precise, clear level of gradated display to the liquid crystals by presenting a digital gradated display rather than a conventional [analogue] analog gradated display.

In order to obtain a [good] quality gradated picture, the drive frequency of the drive IC is raised [and], the frame frequency is not reduced substantially and the frame frequency does not fall below the visually discernable minimum frequency (the lowest confirmed number of frames) in the method of displaying a gradated image, in accordance with the present invention.

[With] In accordance with the present invention, a gradated display is provided in an active-matrix-type liquid crystal display device[, using]. The display uses a display drive system with [the] a display timing related to the unit time t for writing-in a picture element and to the time F for writing-in one picture[, wherein, by]. By time-sharing the signal during a write-in of time t, without changing the time F, a gradated display corresponding to the ratio of the division is obtained since an average electric field applied to a liquid crystal at a picture element (pixel) during the time t can be controlled by controlling the ratio of the division.

For purposes of explanation, [the type of] a 4 x 4 matrix shown in FIG. 3 will be used in discussing the present invention. In the case of a method for gradated display with a conventional display device, as shown in FIG. 4, the electric fields like 220-223 to be applied to the pixel electrodes are determined depending on the strength of the electric fields to the signal lines 210-213 of the data electrode direction, from which the transmittance of the liquid crystals is determined. Note reference numerals in Fig.3 corresponds to that in Fig.4.

In the present invention, [this type of analogue] analog gradation control is not used, and the signal during a write-in unit time t 225 for writing in a pixel is time-shared as shown in FIG. 1[,]. This is done so that the gradated display can be [accomplished] achieved with each of the divisions used as a minimum unit.

At this time, in the case where the electric fields 227, 229, 231 in the write-in time are changed as shown in FIG. 1, the electric fields in the non-write-in time become the average values 228, 230, 232, and a clear gradated display becomes possible.

For another explanation, [the type of] a 2x2 matrix shown in Fig.10 or Fig.17 will be used in discussing the present invention. In another method for gradated display with a conventional display device, as shown in Fig.11, a plurality of picture frames, [for example,] (e.g., 16 frames) are used, and the electric field over the picture element electrodes is determined as the average voltage for 16 frames by turning the picture elements ON and OFF, from which the transmittance of the liquid crystals is determined.

In the present invention, however, the conventional [analogue] analog gradation control or the gradated display with

a plurality of frames is not used, and the signal during a write-in unit time t 325 for writing in a pixel is time-shared as shown in Fig.9 and Fig.16, so that the gradated display can be accomplished with each of the divisions used as a minimum unit. In the case of the circuit shown in Fig.10, a gradated display can be obtained with the signal in Fig.9[, and in]. In the case of the circuit shown in Fig.17, a gradated display is obtained with the signal in Fig.16.

At this time, in the case where the electric fields 327, 329 in the write-in time are changed as shown in Fig.9 or Fig.16, the liquid crystals are activated by the average value of the applied voltage and a clear gradated display becomes possible.

In another method of the present invention, a digital gradated display is [carried out] achieved without changing the frame frequency and with the data transfer frequency and the frequency for gradated display being independent of each other.

In the case of a liquid crystal electro-optical device having 1920x400 dots, for example, the data transfer on the information signal side by 8 bit parallel transfer requires [the] a clock frequency of 5.76MHz. If the conventional method with a plurality of frames, e.g. 10 frames, is employed for this data transfer, the clock frequency as high as 57.6MHz is necessary. However, since the clock frequency for a gradated display is made independent in the present invention, a gradated display having about 166 gradations is possible with an IC driven at 8MHz in maximum. If an IC driven at 12.3MHz is used, a display having 256 gradations, which is considered necessary for a visual display, is sufficiently possible. Therefore, the gradated display in accordance with the above method is greatly advantageous over the conventional [analogue] analog gradated display and the gradated display with a plurality of frames.

Liquid crystal components which can be utilized in the present invention are a material exhibiting ferroelectricity, a material exhibiting anti-ferroelectricity, a material consisting mainly of a nematic liquid crystal, a material consisting mainly of a cholesteric liquid crystal, a nematic liquid crystal dispersed in an organic resin, a cholesteric liquid crystal dispersed in an organic resin, and a smectic liquid crystal dispersed in an organic resin.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 [is] illustrates a graph showing an example of the drive waveforms in this invention;

Fig. 2 [is] illustrates a graph showing the electro-optical characteris-tics of the nematic liquid crystal;

Fig. 3 [is] illustrates an electric circuit of the NTFT matrix;

Fig. 4 [is] illustrates a graph showing an example of the drive waveforms in the prior art device;

Fig. 5 [is] illustrates a partly cut-away plan view of the device of an embodiment in the present invention;

Figs. 6 (A) to 6 (G) are cross-sectional views to show the manufacturing process of an example of this invention;

Fig. 7 shows examples of picture elements in display in this invention;

Fig. 8 shows another example of the drive waveforms in this invention.

Fig.9 [is] illustrates a graph showing an example of the

drive waveforms in accordance with the present invention;

Fig.10 shows an example of the circuit configuration of a liquid crystal electro-optical device in accordance with the present invention;

Fig.11 [is] illustrates a graph showing another example of conventional drive waveforms;

Fig.12 shows a layout of electrodes and the like of one embodiment of the present invention;

Figs. 13(A) to 13(F) [are] illustrate cross-sectional [view] views to show the formation process of a substrate of the present invention;

Fig.14 [is] illustrates a gradated display obtained in one embodiment of the present invention;

Fig.15 [is] illustrates a graph showing another example of the drive waveforms in the present invention.

Fig.16 [is] illustrates a graph showing another example of the drive waveform in accordance with the present invention;

Fig.17 is another example of the circuit configuration of a liquid crystal electro-optical device of the present invention;

Figs. 18 (A) to 18(F) are cross-sectional views to show the formation process of a substrate of one embodiment of the present invention;

Fig.19 [is] illustrates a graph showing an example of the drive waveforms in the present invention;

Fig.20 shows gate voltage-drain current characteristics in a polycrystalline silicon TFT and an amorphous silicon TFT.

Fig.21 [is] illustrates another example of the circuit configuration of a liquid crystal electro-optical device of the

present invention;

Figs.22(A) to 22(I) are cross-sectional views to show the manufacturing process of another example of the present invention;

Figs.23(A) to 23(E) are cross-sectional views to show the formation process of a substrate of the present invention;

Fig.24 shows a schematical configuration of an electro-optical device of one embodiment of the present invention;

Fig.25 shows the peripheral circuitry of a liquid crystal electro-optical device of the present invention;

Figs.26(A) to 26(E) are cross-sectional views to show the manufacturing process of a liquid crystal device of one embodiment of the present invention;

Fig.27 shows an assembly of a projection type image display of one embodiment of the present invention;

Figs.28(A) to 28(G) are cross-sectional views to show the manufacturing process of a liquid crystal display device of one embodiment of the present invention;

Fig.29 shows a schematic configuration of a liquid crystal electro-optical device of one embodiment of the present invention;

Fig.30 shows a schematic configuration of a reflection type liquid crystal dispersion display device of one embodiment of the present invention;

Fig.31 [is] illustrates an example of the circuit configuration of a liquid crystal display device of the present invention;

Fig.32 [is] illustrates a layout of electrodes and the like

of another embodiment of the present invention;

Figs.33(A) to 33(H) are cross-sectional views to show the manufacturing process for a liquid crystal panel of one embodiment of the present invention;

Fig.34 shows the peripheral circuitry of a liquid crystal electro-optical device of the present invention;

Figs.35(A) to 35(D) are graphs showing input signal waveforms inputted to and output signal waveforms outputted from the C/TFT obtained in one embodiment of the present invention;

Figs.36(A) to 36(G) are cross-sectional views to show the manufacturing process for a liquid crystal display device of one embodiment of the present invention;

Fig.37 [is] illustrates a layout of electrodes and the like of another embodiment of the present invention;

Fig.38 [is] illustrates a layout of electrodes and the like of still another embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS[

[Embodiment 1]

]

In [this] a first embodiment of the present invention, a liquid crystal display device with the circuit configuration shown in FIG. 17, [that is](i.e., a buffer type circuit configuration) is used. FIG. 38 shows the layout of the actual electrodes and the like corresponding to the circuit configuration of FIG. 17. In order to simplify the explanation, the parts corresponding to a 2x2 matrix only are described. [Also, the actual] The driving signal waveform is shown in FIG.

16. For simplicity, the explanation of the signal waveform is also given for the case of 2x2 matrix configuration.

The manufacturing process for forming the substrate for the liquid crystal display device used in an embodiment of the present invention is shown in [FIG. 18] Fig. 18(A)-18(F). In Fig. 18(A), a silicon oxide film for a blocking layer 951 having a thickness of 1000 to 3000 angstroms [was] is formed on a glass substrate 950, using a magnetron RF (high frequency) sputtering method. The glass substrate 950 [was] is made of inexpensive glass capable of withstanding heat treatment up to 700 °C e.g. of 600 °C.

The process conditions [were] are as follows:

atmosphere: 100% oxygen;

film forming temperature: 150 °C;

output: 400 to 800 W; and

pressure: 0.5 Pa.

The film forming, using either quartz or single-crystal silicon for a target [had] has a speed of 30 to 100 Angstroms/minute.

On top of this construction, an amorphous silicon film [was] is formed using an LPCVD (low pressure chemical vapor deposition) method, sputtering method, or a plasma CVD method.

If using the LPCVD method to form the silicon film, disilane (Si_2H_6) or trisilane (Si_3H_8) [was] is supplied to the CVD apparatus at a temperature 100 to 200 °C less than the crystallization temperature[, that is] (i.e., 450 to 550 °C, for example at 530 °C). The pressure inside the reaction furnace [was] is 30 to 300 Pa. The film forming speed [was] is 50 to 250

Å/minute. In order to control the threshold voltage (Vth) of both the NTFT and PTFT at a substantially same level, boron with a concentration of $1x10^{15}$ to $5 \times 10^{18}cm^{-3}$ can be added using diborane. [In the case of] If using a sputtering method, the conditions [were] are as follows[;]:

back pressure before sputtering: up to $1x10^{-5}$ Pa;

target: a single crystal silicon;

atmosphere: argon with hydrogen 20 to 80% by volume

e.g. 20 volume % Ar and 80 volume % H_2;

the film forming temperature: 150 °C;

frequency: 13.56 MHz;

sputter output: 400 to 800W; and

pressure: 0.5 Pa.

[In the case of] When forming a silicon film using the plasma CVD method, the temperature [was] is 300 °C for example, and monosilane (SiH_4) or disilane (Si_2H_6) [was] is used as the reactive gas, which [were] are input into a PCVD apparatus and 13.56 MHz high frequency electric power [was] is applied for film forming.

[In this method, it is preferable that] Preferably, the oxygen concentra-tion of the film formed is $5x10^{21}cm^{-3}$ or less. If the oxygen concentration is higher than this range, crystallization becomes difficult and the heat annealing temperature must be high or the annealing time long. On the other hand, if the concentration is too low, the current leak in the OFF state increases because of the back light. For this reason the concentration is held in the range from 4×10^{19} to $4x10^{21}cm^{-3}$. [Silicon] The silicon concentration [was] is assumed to be $4 \times 10^{22}cm^{-3}$ and hydrogen concentration [was] is $4 \times 10^{20}cm^{-3}$, which is

equal to one atomic % of the silicon concentration.

Also, to promote further crystallization at the source and drain, the oxygen concentration is adjusted to 7 x $10^{19}cm^{-3}$ or less, or, preferably, $1x10^{19}cm^{-3}$ or less, and oxygen may be added by ion implantation to a concentration range of $5x10^{20}$ to $5x10^{21}cm^{-3}$, only to the channel forming regions of the TFTs which form the pixels. On the other hand, it is effective for a high frequency operation to reduce the amount of oxygen contained in the TFT provided in the peripheral circuits which no light reaches, so as to make the carrier mobility greater.

After the amorphous silicon film [was] is formed to a thickness of 500 to 5000 Å, for example 1500 Å by means of the foregoing process, an intermediate heat treatment [was] is performed at 450 to 700 °C for 12 to 70 hours in an oxygen-free atmosphere, for example, in a hydrogen atmosphere at 600 °C.

Because an amorphous silicon oxide film [was] is formed on the surface of the substrate, beneath the silicon film, no specific nucleus [existed] exists in this heat treatment, so the whole amorphous silicon film [was] is uniformly heat annealed. Specifically, the amorphous structure [was] is kept in film forming and hydrogen [was] is merely mixed in.

[It was supposed that when] When annealing the silicon film, [crystallization was] crys-tallization is inclined to take place in a highly ordered state from the amorphous structure, so that a crystal state [was] is partly produced. Particularly, in the regions where a relatively highly ordered state [was] is produced just after film forming of silicon, the tendency of crystallization to a crystal state [was] is strong. A junction, however, [took] takes place due to the silicon located between these regions, so that the silicon attracted each other.

According to laser Raman spectrometry measurement of the annealed silicon film, [it was observed that] a peak [thereof was] is shifted from 522cm^{-1} of the single crystal silicon to a lower frequency side. The apparent grain diameter, when calculated using the half-value width, [was] is 50 to 500 Å, like a micro crystal. Actually, [there were] many of these highly crystallized regions [that made] make up clusters. Each cluster [was] is joined to the other by a silicon junction [(anchoring)] forming (i.e., anchoring) a semi-amorphous film.

Consequently, it [was] is believed that the film could be said to have substantially no grain boundary (GB). The carriers [could] can easily travel between the clusters through the anchored areas, so that the mobility of the carriers [was] is higher than that of the poly-crystalline silicon having clear grain boundaries (GB). The Hall mobility obtained [was] is (μh)=10 to 200cm^2/Vsec, and the electron mobility obtained [was] is (μe)=15 to 300cm^2/Vsec.

When the film is polycrystallized at a higher temperature of 900 to 12000 °C and not an intermediate temperature, as described above, segregation of impurities occurs due to the growth of solid phase from nucleus in the film, and there are a lot of impurities such as oxygen, carbon, nitrogen in GB. Therefore, the mobility is large in the crystal, but the movement of carriers is prohibited by the barrier at GB. Consequently, it is actually impossible to obtain the mobility of 10cm^2/Vsec. or more.

This is [a] one reason why a silicon semiconductor with a [semia-morphous] semi-amorphous or semicrystalline structure is used in this embodiment. Of course, other crystalline semiconductor materials having a high mobility can also be used in the present invention. FIG. 18(A) shows the silicon film which [was] is photoetched using a first photomask 91, with the NTFT

region 913 (20 um in channel width) prepared at the left side of the drawing and the PTFT region 922 at the right side.

A silicon oxide film [was] is then formed as a gate insulation film in the thickness range of 500 to 2000 Å[, for example,] (e.g., 1000 Å). This is prepared under the same conditions as the silicone oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ion during film forming.

When this operation [was] is completed, a silicon film [was] is provided containing a 1 to 5 x $10^{21}cm^{-3}$ concentration of phosphorus. Molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film may be optionally formed on this silicon film to form a multilayer film. The silicon film (or multilayer film) [was] is patterned with a second photomask 92 to obtain the configuration shown in FIG. 18(B). An NTFT gate electrode 909 and a PTFT gate electrode 921 [were] are then formed. For example, as a gate electrode, a phosphorus-doped silicon 0.2μm thick [was] is formed and a molybdenum layer 0.3 μm thick [was] is formed thereon with a channel length of 10μm.

As shown in FIG. 18(C), a photoresist 957 [was] is formed using a photomask 93 , and boron [was] is added using the ion implantation method at a dosage of 1 to 5 x $10^{15}cm^{-2}$ for the PTFT source 918 and drain 920. Next, as illustrated in FIG. 18(D), a photoresist 961 [was] is formed using a photomask 94. Phosphorous [was] is added using the ion implantation method at a dosage of 1 to 5 x $10^{15}cm^{-2}$ for an NTFT source 910 and drain 912.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the second photomask 92, it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface

of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The doping above is made through a gate insulation film 954. However, in FIG. 18(B), using the gate electrodes 921, 909 as a mask, the silicone oxide on the silicone film may be removed[,] followed by the addition of the boron and phosphorous directly into the silicon film using the ion implantation method.

Next, annealing [was] is again conducted for 10 to 50 hours at 600 °C. The impurities of the NTFT source 910 and drain 912, and the PTFT source 918, and drain 920, [were] are activated to form P+ and N+ regions. The channels 919 and 911 below the gate electrodes 921 and 909 [were] are made of a semi-amorphous semiconductor.

The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above 700 °C in the self-aligning system. This makes it possible to use [other] materials other than expensive quartz as the substrate material. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large picture element.

The heat anneal process, shown in Fig. 18(A) and Fig. 18(D), [was] is performed twice. However, the anneal process of Fig. 18(A) can be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig. 18(D), thereby shortening the manufacturing time. Also, in Fig. 18(E), the interlayer insulation layer 965 [was] is made of silicon oxide film using the sputtering method mentioned above.

This silicon oxide film can, however, also be formed using the LPCVD method or photo CVD method or normal pressure CVD

method. The thickness of the insulation layer [was] is e.g. 0.2 to 0.6μm.

Next, using photo mask 95 , a window 966 for the electrodes [was] is formed. Then, a layer of aluminum [was] is formed over the entire structure using the sputtering method, and leads 971 and 972 and contacts 967, 968 [were] are made using photo mask 96. An organic resin film 969 for surface-flattening, e.g. a transparent polyimide resin film [was] is formed, and electrode open-ings [were] are provided using photomask 97.

Two TFTS [were] are formed in a complementary structure in a picture element of the liquid crystal display device as shown in FIG. 18(F) [, in which the]. The output [terminal] terminals of the TFTS [was] are each connected to the (transparent) electrode of the picture element of the liquid crystal display device, forming the ITO (Indium Tin Oxide) by sputtering. The electrode 917 [was] is completed by etching through the photomask 98.

[This] The ITO film [was] is formed in the range from room temperature to 150 °C and finished by annealing at 200 °C to 400 °C in oxygen or atmosphere. The NTFT 913, the PTFT 922 and the transparent electrode 917 [were] are thus prepared on a single glass substrate 950.

The electrical characteristics of the TFT obtained thus are as follows:

mobility in the PTFT: 20cm^2/Vs;

Vth in the PTFT: -5.9 V;

mobility in NTFT: 40cm^2/Vs; and

Vth in NTFT: 5.0 V.

Another glass substrate, provided with a transparent electrode over the entire surface thereof, and the substrate

fabricated according to the above-described method [were] are combined to form a liquid crystal cell. A TN liquid crystal material [was] is injected into the liquid crystal cell. FIG. 38 illustrates the positioning of the electrodes and the like for the liquid crystal display device according to this embodiment.

An NTFT 913 is provided at the intersection of a first signal line 905 and a third signal line 903, and, in the same manner, an NTFT for another picture element is provided at the intersection of the first signal line 905 and a third signal line 904. A PTFT is provided at the intersection of a second signal line 908 and the third signal line 903. Also, an NTFT for another picture element is provided at the intersection of another, adjacent first signal line 906 and the third signal line 903, while in the same manner an NTFT is provided at the intersection of the first signal line 906 and the third signal line 904.

The NTFT 913 is connected to the first signal line 905 through a contact on the input terminal on the drain 910, and the gate 909 is connected to a signal line 903 which is formed of multilayer wiring. The output terminal of the source 912 is connected to a picture element electrode 917 through a contact.

The PTFT 922 is connected to the second signal line 908 through a contact on the input terminal on the drain 920, wherein the gate 921 is connected to the signal line 903, and the output terminal of the source 918 is connected to the picture element electrode 917 through a contact in the same way as in the NTFT.

[Adjacently, another] An adjacent C/TFT [which] is connected to [the same] signal line 903 [is provided], and the PTFT 922 of [said another] the C/TFT is connected to a second signal line 907[, and]. Also, the NTFT 913 of [said another] the adjacent C/TFT is connected to the first signal line 906.

One pixel comprising a picture element 923, formed from a transparent conducting film and a C/TFT, is interposed between this pair of signal lines 905 and 908. By repeating this type of configuration laterally and vertically, the 2x2 matrix can be expanded to form a large picture element liquid crystal display device of 640x480 or 1280x960 matrixes.

A special feature of [this] the device of the present invention is that the picture element electrode 917 is set at three values of the liquid crystal poten-tial V_{LC} by providing a complementary configuration of two TFTs for one picture element.

Next, in order to form a second substrate, an ITO film (Indium Tin Oxide) [was] is formed by sputtering on a substrate which [was] is formed by laminating a silicon oxide film to a thickness of 2000 Å on glass plate by the sputtering process. This ITO film [was] is formed in the range from room temperature to 150 °C and fin-ished by annealing at 200 °C to 400 °C in oxygen or atmosphere.

A polyimide precursor member [was] is printed on the above-mentioned substrate using the offset method and fired for one hour at 350 °C in an oxygen-free atmosphere (for example, in a nitrogen atmosphere). The polyimide surface [was] is then reformed using a commonly known rubbing method, so that a means for orienting the liquid crystal molecules in a uniform direction in at least the initial stage [was] is provided, whereby the second substrate [was] is completed.

[Then] Next, the liquid crystal composition, having ferroelectricity [was], is interposed between the first and second substrates, and the assembly [was] is sealed around the periphery using an epoxy-type adhesive. A drive IC of a TAB form [was] is connected to a lead on the substrate and a polarizing

plate [was] is affixed to the outside to obtain a light-transmission type of liquid crystal display device.

FIG. 14 shows the display for the A, E, and C picture elements when the drive waveform shown in FIG. 16 is applied. In Fig.14, darkness is expressed by a dot. A clear gradated display is obtained, as shown in Fig.14.

[[Embodiment 2]

In this] In a second embodiment of the present invention, a first substrate and a second substrate [were] are obtained using the same process as for the Embodiment 1. However, no polyimide film for alignment [was] is formed on the second substrate. Since this device [was] is made for use in a video camera viewfinder, the pitch of the picture element [was] is 60μm, and a matrix 200 high x300 wide [was] is formed.

In this embodiment, a nematic liquid crystal composition [was] is dispersed throughout an acrylic organic resin to form a dis-persed-type liquid crystal display device. 62 wt% of the nematic liquid crystals [was] is dispersed throughout an acrylic resin dena-tured with an ultraviolet-curable epoxy. This material [was] is interposed between the first and second substrates, and is then cured by the application of a light beam from a UV light source with a 1000 mW output for 20sec.

This display device [was] is time-shared into 16 separate time periods to provide a gradated display, and each color [had] has 16 gradations, to give a liquid crystal display device which can display a total of 4096 colors. The drive wave form at that time is shown in FIG. 19.

In summary, a plurality of write-in entries (display frames) is provided in conventional gradated display methods. For example, 16 frames are utilized to provide a method for presenting a

gradated display by a combination of their ON/OFF states. If, in a total 16 frames, eight frames are ON and the remaining eight frames are OFF, a gradated display results at a 50% transmission, which is the average transmittance in this case. If, however, four frames are ON and the remaining 12 frames are OFF, the average transmittance becomes 25% and a gradated display occurs at this transmission.

When this conventional method is used, there is a strong possibility [of] that the number of frames is less than the lowest con-firmed number of frames[, 30 frames,] (30 frames) which [are] is the minimum number of frames that can be discerned by the human eye. This is the main cause of a drop in the quality of the display.

In this embodiment, where the frequency of the driver is increased [for providing] to provide a gradated display [of] in accordance with the present invention, a gradated display becomes possible preventing the actual frame frequency from decreasing. Therefore, the frequency is never [becomes] lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality picture can be provided.

By using the same type of process and drive method it is possible to provide a word processor screen, a computer screen, or a device for projecting a visual image display.

[[Embodiment 3]

]The liquid crystal electro-optical device utilized in [this] a third embodiment of the present invention has the circuit configuration shown in Fig.10, namely, the circuit configuration of inverter type. FIG. 12 shows the layout of the actual electrodes and the like corresponding to the circuit

configuration of FIG.10. In order to simplify the explanation, the parts corresponding to a 2x2 matrix only are described. Also, the actual driving signal waveform is shown in Fig.9.

The process for forming a substrate for the liquid crystal electro-optical device utilized in this embodiment is shown in Figs.13(A) to (F). In accordance with the process shown in Figs. 13(A) to (F), the substrate shown in Fig.13(F) [was] is formed in the same manner as in Embodiment 1. The substrate [had] has the same structure as that in Embodiment 1 except that the location of a PTFT and an NTFT thereof [was] is opposite to that of Embodiment 1, as shown in Figs.10 and 13. With [thus] the obtained substrate, a light-transmission type liquid crystal electro-optical device [was] is completed as in Embodiment 1.

[[Embodiment 4]

In this] In the fourth embodiment of the present invention, a first substrate and a second substrate [were] are obtained using the same process as [for Embodiment 3] described with respect to the third embodiment. However, an orientation film made of polyimide [was] is not formed on the second substrate. With these first and second substrates, a liquid crystal electro-optical device for use in a video camera viewfinder [was] is formed at a pitch of a picture element of 60 μm, and a matrix 200 high x300 wide in the same way as in Embodiment 2.

In this embodiment, where the frequency of the driver is increased for providing a gradated display of the present invention, a gradated display becomes possible, preventing the actual frame frequency from decreasing. Therefore, the frequency never becomes lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality

picture can be provided.

By using the same type of process and drive method it is possible to provide a word processor screen, a computer screen, or a device for projecting a visual image display.

In the drive method of the present invention shown in Fig.15 where the unit time [t 225] t_{225} for writing-in a picture element is [devided] divided into 16 minimum units (a period of each minimum unit 227 is t/16), each color is displayed with 16 gradations, so that a display with 4096 colors is possible in total.[

[Embodiment 5]

]

In [this] the fifth embodiment of the present invention, a liquid crystal display device with the circuit configuration shown in FIG. 3 is used. FIG. 5 shows the layout of the actual electrodes and the like corresponding to the circuit configuration of FIG. 3. In order to simplify the explanation, the parts corresponding to a 4x4 matrix (2x2 matrix) only are described. Also, the actual driving signal waveform is shown in FIG. 1. For simplicity, the explanation of the signal waveform is also given for the case of 4x4 matrix configuration.

The manufacturing process for the liquid crystal display device used in this embodiment is shown in [FIG. 6] Figs. 6(A)-6(D). In Fig. 6(A), a silicon oxide film for a blocking layer 51 having a thickness of 1000 to 3000 angstroms [was] is formed on a glass substrate 50, using a magnetron RF (high frequency) sputtering method. The glass substrate 50 utilized [was] is the one which [was] is not expensive unlike quartz glass and [was] is resistant to heat treatment up to 700 °C e.g. of 600 °C. The conditions for the process are as follows:

Atmosphere: 100% oxygen;

Film Formation Temperature: 150 °C;

Output Power: 400-800W; and

Pressure: 0.5Pa.

The film formation, using either quartz or single-crystal silicon for a target, [had] has a speed of 30 to 100 Å/min.

On the top surface thereof, a silicon film in an amorphous state having a thickness of 500 to 5000 Å, e.g. 1500 Å, [was] is formed as in Embodiment 1. In the case of using low pressure CVD method to form the amorphous silicon film as in Embodiment 1, boron may be added at a concentration of $1x10^{15}$ to $1x10^{18}cm^{-3}$ by the use of diborane during the film formation, in order to control the threshold voltage (Vth) of the NTFT.

Then, in the same manner as in Embodiment 1, the silicon film in an amorphous state [was] is heat-annealed at an intermediate temperature of 450 to 700 °C for 12 to 70 hours under a non-oxide atmosphere. Then, an NTFT region 13 [was] is obtained from the silicon film by the use of a first photomask 1 .

A silicon oxide film [was] is then formed as a gate insulating film 54 in the thickness range of 500 to 2000 Å[, for example,] (e.g., 1000 Å). This is prepared under the same conditions as the silicone oxide film formed as a blocking layer. A small amount of fluorine may be added to the film for fixation of the sodium ion during the film formation.

When this operation [was] is completed, a silicon film containing a 1 to $5x10^{21}cm^{-3}$ concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film [was] is formed[, which was]. The film is then patterned with a second

photomask 2 to obtain the configuration shown in FIG. 6(B). Phosphorus [was] is added by ion implantation method at a dosage of 1 to $5x10^{15}cm^{-2}$ for a NTFT source 20 and drain 18, using the gate electrode 9 as a mask.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the second photomask 2 , it is possible to form [the] source and drain contact holes at positions closer to the gate by anodic oxidation of [this] the surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The above-described process is carried out through the gate insulating film 54. However, as illustrated in FIG. 6(B), it is possible to remove the silicon oxide formed on the silicon film using the gate electrode 9 as a mask and then add the phosphorus directly into the silicon film using the ion implantation method.

Next, annealing [was] is again conducted for 10 to 50 hours at 600 °C. The impurities [were] are activated whereby the source 20 and drain 18 of the NTFT [were] are made N^+ regions. A channel forming region 21 of semi-amorphous semiconductor [was] is formed below the gate electrode 9.

The entire manufacturing process for the NTFT can thus be done without having to apply a temperature above 700 °C in spite of the self-aligning system. [This makes] Thus, it is possible to use materials other than expensive ones such as quartz for the substrate material. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of pixels.

The heat anneal process [was] is carried out twice as shown

in Figs. 6(A) and (C). However, the anneal process of Fig. 6(A) may be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig. 6(C), thereby shortening the manufacturing time. Also, in Fig. 6(D), the interlayer insulating layer 65 [was] is made of silicon oxide film using the sputtering method mentioned above.

[This] The silicon oxide film can, however, also be formed using the LPCVD method or photo CVD method or normal pressure CVD method. The thickness of the film [was] is e.g. 0.2 to 0.6 μm.

Next, using photo mask 3 , an opening 66 for the electrodes [was] is formed. Then, a layer of aluminum [was] is formed on the entire surface by sputtering, and leads 71 and 72 and contacts 67, 68 [were] are formed by using photo mask 4. [ ]An organic resin film 69 for surface-flattening, e.g. a transparent polyimide resin film [was] is formed, and openings for electrodes [were] are provided using a photomask 5.

The TFT [was] is thus formed as shown in FIG. 6(F), and further an ITO (Indium Tin Oxide) film [was] is formed by sputtering [in order] so that the output terminal of the TFT [was] is connected to a transparent electrode of the picture element of the liquid crystal display device by the ITO.

The electrode [was] is completed by etching the ITO film through a photomask 6 , whereby a pixel electrode 17 and a contact 73 of the pixel electrode with the drain electrode [were] are completed. This ITO film [was] is formed in the range from room temperature to 150 °C and annealed at 200 °C to 400 °C in oxygen or atmosphere.

The NTFT 13 and the transparent pixel electrode 17 [were] are thus prepared on an identical glass substrate 50. [ ]The electrical characteristics of the TFT [thus] formed are as

follows:

mobility: 40cmcm^2/Vs; and

Vth: 5.0V.

The first substrate [was thus] is thereby completed.

[Then, a] A second substrate [was] is manufactured in the same manner as the second substrate of the first embodiment. Next [Embodiment 1. Then], the liquid crystal composition exhibiting ferroelectricity [was] is interposed between the first and second substrates, and the assembly [was] is sealed around the periphery using an epoxy-type adhesive. A drive IC of a TAB form [was] is connected to a lead on the substrate and a polarizing plate [was] is affixed to the outside to obtain a light-transmission type of liquid crystal display device.

FIG. 7 shows the display for the A, F, and I picture elements when the drive waveform shown in FIG. 1 is applied. [This figure] Figure 7 additionally shows that a clear gradated display is obtained.[

[Embodiment 6]

]

In [this] a sixth embodiment of the present invention, a first substrate and a second substrate [were] are obtained using the same process as for [Embodiment 5] the fifth embodiment. However, an orientation film made of polyimide [was] is not formed on the second substrate. With these first and second substrates, a liquid crystal electro-optical device for use in a video camera viewfinder [was] is formed at a pitch of a picture element of 60 μm and a matrix 200 high x300 wide in the same way as in [Embodiment 2] the second embodiment of the present invention.

In the drive method of the present invention shown in Fig.8, where the unit time t for writing-in a picture element is [devided] divided into 16 minimum units (a period of each minimum unit is t/16), each color is displayed with 16 gradations, so that a display with 4096 colors is possible in total.

In this embodiment, where the frequency of the driver is increased for providing a gradated display of the present invention, a gradated display becomes possible, thereby preventing the actual frame frequency from decreasing. Therefore, the frequency never becomes lower than a visually confirmed frequency, so that a drop in display quality does not occur, and a high quality picture can be provided.

[It is effective to improve the ability of gradated display over the conventional one by conducting] The quality of gradated displays can be improved over conventional displays by performing the above-mentioned conventional method for gradated display together with the method for gradated display in accordance with the present invention. The method of the present invention is to control the average voltage applied to a liquid crystal pixel, where complete response of liquid crystal is not required.

Conventionally, it was difficult to directly apply the voltages V_b and V_c shown in Fig.2 to pixels. However, by changing the average of the voltage applied to pixel electrodes, an effect can be obtained as if the voltages V_b and V_c [were] are directly applied to pixels.

In other words, the present invention [is to provide] provides a method for controlling liquid crystal which responds incompletely. Although only N-channel field effect transistors are utilized in this embodiment, P-channel field effect

transistors may also be utilized. [instead.

[Embodiment 7]]

In [this] the seventh embodiment of the present invention, a liquid crystal electro-optical device (image display device) with the circuit configuration shown in Fig.21 is utilized as a television to be [hanged] placed on [the] a wall, for example. The TFTs utilized therein are made of polycrystal silicon subjected to laser annealing and are of stagger type.

Referring to Fig.21, [a reference numeral 700 designates] a gate electrode[, 701] 700, a source[, 702] 701, a drain[, 703] 702, a NMOSTFT 703, and [704] a pixel electrode 704 are shown. Also illustrated in Fig. 21 is a lead contact 705 and a pixel contact 706. The layout of the actual electrodes and the like corresponding to the circuit configuration in Fig.21 is shown in Fig.37. [For simplifying] To simplify the explanation, the parts corresponding to a 2x2 (or less) matrix only are described. Also, the reference numerals are made so as to correspond to those in Fig.21. [The reference numeral 705 designates a lead contact and 706 a pixel contact.]Further, the actual driving signal waveform is shown in Fig.1. For simplicity, the explanation of the signal waveform is also given for the case of 4x4 matrix configuration.

The manufacturing process for the liquid crystal display device used in this embodiment is shown in [FIG.22] Figs. 22(A)-22(I). In Fig.22(A), a silicon oxide film for a blocking layer 801 having a thickness of 1000 to 3000 angstroms [was] is formed on a glass substrate 800, using a magnetron RF (high frequency) sputtering method. The glass substrate 800 utilized [was] is the one which [was] is not expensive unlike quartz glass and [was] is resistant to heat treatment up to 700 °C e.g. of 600 °C. The

conditions for the process are as follows:

Atmosphere: 100% oxygen;

Film Formation Temperature: 150 °C;

Output Power: 400 - 800W; and

Pressure: 0.5Pa.

The film formation, using either quartz or single-crystal silicon for a target, [had] has a speed of 30 to 100 Å/min.

On [this] the silicon oxide film, a silicon film in an amorphous state [was] is formed. In the case of using plasma CVD method to form this amorphous silicon film, the film formation temperature [was] is from 250 °C to 350 °C[,] (e.g. 320 °C in this embodiment), and monosilane (SiH_4) [was] is utilized. However, disilane (Si_2H_6) or trisilane (Si_3H_8) may be utilized instead of monosilane. The gas [was] is inputted to a PCVD apparatus, maintained at a pressure of 3 Pa and a high frequency electric power [was], is applied thereto at a frequency of 13.56 MHz, whereby the silicon film [was] is deposited. A high frequency electric power of 0.02 to 0.10W/cm^2 [was] is appropriate in this case, and in this embodiment a high frequency electric power of 0.055W/cm^2 [was] is applied. The flux of the monosilane [was] is at 20SCCM and the film formation rate under this condition [was] is about 120 Å/min.

Boron may be added at a concentration of $1x10^{15}$ to $1x10^{18}cm^{-3}$ by using diborane during the film formation, in order to control the threshold voltage (Vth) of the NTFT.

Not only this plasma CVD method but also sputtering method and low pressure CVD method can be utilized for forming the silicon film to be a channel region in a TFT. In the case of using a sputtering method, the conditions [were] are as follows:

back pressure before sputtering: up to $1x10^{-5}$ Pa;

target: a single crystal silicon;

atmosphere: argon with hydrogen 20 to 80% by volume,

e.g. 20 volume % Ar and 80 volume % H_2;

the film forming temperature: 150 C;

frequency: 13.56 MHz;

sputter output: 400 to 800W; and

pressure: 0.5 Pa.

If using the LPCVD method to form the silicon film, disilane (Si_2H_6) or trisilane (Si_3H_8) [was] is supplied to the CVD apparatus at a temperature 100 to 200 °C less than the crystallization temperature[, that is] (i.e., 450 to 550 °C, for example at 530 °C). The pressure inside the reaction furnace [was] is 30 to 300 Pa. The film forming speed [was] is 50 to 250 Å/minute.

With respect to the film formed by these methods, it is preferable that the oxygen concentration is $5x10^{21}cm^{-3}$ or less. In order to promote crystallization of the film, it is desirable that the oxygen concentration is $7x10^{19}cm^{-3}$ or less, preferably $1x10^{19}cm^{-3}$ or less. However, if the concentration is too low, the current leak in the OFF state increases because of the back light. If the oxygen concentration is too high, crystallization becomes difficult and the laser annealing temperature must be increased or the annealing time lengthened. [Silicon] The silicon concentration [was] is assumed to be $4x10^{22}cm^{-3}$ and the hydrogen concentration [was] is $4x10^{20}cm^{-3}$ which is equal to one atomic % of the silicon concentration.

Also, to promote further crystallization at the source and drain, the oxygen concentration is adjusted to $7x10^{19}cm^{-3}$ or less,

or, preferably, $1x101^{19}m^{-3}$ or less, and oxygen may be added by ion implantation to a concentration range of $5x10^{20}$ to $5x10^{21}cm^{-3}$, only to the channel forming regions of the TFTs which form the pixels.

By the above-described method, the silicon film 802 in an amorphous state [was] is formed to be 500 to 5000 Å in thickness, [e.g.] (e.g., 1000 Å in this embodiment).

[Then,] Next, photoresist 803 [was] is formed in a pattern having openings therein on source and drain regions as shown in Fig.22(B) by the use of a mask 1 . On this structure, a silicon film 804 to be an n-type activation layer [was] is formed by plasma CVD. The film formation temperature [was] is 250 °C to 350 °C[,] (specifically 320 °C in this embodiment). Monosilane (SiH_4) and phosphine (PH_3) of monosilane base at a concentration of 3% [were] are utilized. They [were] are introduced into a PCVD apparatus maintained at a pressure of 5 Pa and an electric power at a high frequency of 13.56MHz [was] is inputted thereto, whereby the silicon film 804 [was] is deposited. The high frequency electric power of 0.05 to $0.20W/cm^2$ [was] is appropriate in this case[, and in]. In this embodiment an electric power of $0.120W/cm^2$ [was] is inputted.

The n-type silicon film formed by the above-described method [had] has a specific electric conductivity of about $2x10^{-1}[\Omega cm^{-1}]$. The thickness thereof [was] is 50 Å. Then, source and drain regions 805 and 806 [were] are formed by a lift-off method. After that, an island region 807 for an N-channel thin film transistor [was] is formed using a mask 82.

Subsequently, laser annealing to the source, drain, channel regions and laser doping to the activation layer [were] are carried out simultaneously by the use of XeCl excimer laser. The threshold energy of this laser at this moment [was] is $130mJ/cm^2$.

On the other hand, in order to melt the whole film thickness, the energy of 220mJ/cm^2 [was] is necessary. However, if a laser having an energy more than 220mJ/cm^2 [was] is irradiated from the beginning, hydrogen contained in the film would be discharged rapidly, resulting in the [destroy] destruction of the film. For this reason, it is necessary to [firstly] first discharge the hydrogen at a low energy and then melt the film. In this embodiment, a laser at 150mJ/cm^2 [was] is irradiated to discharge hydrogen and then a laser at 230mJ/cm^2 [was] is irradiated to crystallize the film.

[It was supposed that when] When annealing the silicon film, crystallization [was] is inclined to take place in a highly ordered state from the amorphous structure, so that a crystal state [was] is partly produced. Particularly, in the regions where a relatively highly ordered state [was] is produced just after film forming of silicon, the tendency of crystallization to a crystal state [was] is strong. A junction, however, [took place] is created due to the silicon between these regions, so that the silicon attracted each other.

According to laser Raman spectrometry measurement of the annealed silicon film, it [was] is observed that a peak [thereof was] is shifted from 522cm^{-1} of the single crystal silicon to a lower frequency side. The apparent grain diameter, when calculated using the half-value width, [was] is 50 to 500 Å. Actually, there [were] are many of these highly crystallized regions that [made] make up clusters. Each cluster [was] is joined to the other by a silicon junction [(anchoring)] forming (i.e., anchoring) a film.

Consequently, it [was] is believed that the film [could] can be said to have substantially no grain boundary (GB). The carriers [could] can easily travel between the clusters through

the anchored areas, so the mobility of the carriers [was] is higher than that of the poly-crystalline silicon, having clear grain boundaries (GB). The electron mobility (ue) obtained [was] is 15 to 300cm^2/Vsec.

A silicon oxide film 808 [was] is then formed as a gate insulating film in the thickness range of 500 to 2000 Å[, for example,] (e.g., 1000 Å). This is prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ion during film formation.

When this operation [was] is completed, a silicon film containing phosphorus at a concentration of 1 to $5x10^{21}cm^{-3}$ [concentration], or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film [was] is formed. This film [was] is patterned with a third photomask 83 to obtain the configuration shown in FIG. 22(E). A gate electrode 809 [was] is then formed. For example, as a gate electrode, a phosphorus-doped silicon 0.2 μm thick [was] is formed and a molybdenum layer 0.3 μm thick [was] is formed thereon with a channel length of 7 μm.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the third photomask 83 , it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The entire manufacturing process for the TFT can thus be done without having to apply a temperature above 400 °C. This makes it

possible to use, as the substrate, materials other than expensive materials such as quartz. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of picture elements.

[Then] Next, a silicon oxide film [was] is formed as an interlayer insulator 810 by a sputtering method. In place of the sputtering method, a LPCVD method, a photo CVD method, and a normal pressure CVD method may be utilized for the formation of the silicon oxide film. The thickness of the layer [was] is 0.2 to 0.6 μm, for example. After that, an opening 811 for electrode [was] is formed using a forth photomask 84. On the entire surface of this structure, an aluminum film having a thickness of 0.3 μm [was] is formed by sputtering method, and then a lead 812 and a contact 813 [were] are formed using a photomask (85). An organic resin for surface-flattering 814[,] (e.g. a transparent polyimide resin [was]) is then applied on the top surface, and [further] an opening for an electrode [was] is again formed using a sixth photomask 86 .

An ITO (Indium Tin Oxide) film of 0.1 μm thickness [was] is formed on the entire surface of this structure by sputtering and [was] is subsequently patterned into a pixel electrode 815 by using a seventh photomask 87. This ITO film [was] is formed at room temperature to 150 °C and annealed at 200 °C to 400 °C in an oxygen or an atmosphere. The electrical characteristics of the [thus] formed TFT [were] are as follows:

Mobility: 80cm^2/Vs; and

Vth: 5.0V.

In accordance with the foregoing method, the first substrate for a liquid crystal electro-optical device [was] is completed.

The method for forming the second substrate is shown in

[Fig.23] Figs. 23(A)-23(E). A polyimide resin film, made of polyimide mixed with black pigment, having a thickness of 1 μm [was] is formed on a glass substrate 500 by a spin coat method and [was then] is patterned into black stripes 501 by the use of a first photomask 411.

Then, a film of polyimide resin mixed with red pigment having a thickness of 1 μm [was] is formed by spin coat method and [was] is subsequently patterned into red color filters 502 by the use of a second photomask 412.

In the same manner as [the] above, green color filters 503 [were] are formed by the use of a third photomask 413, and blue color filters 504 by the use of a fourth photomask 414. During the formation of the filters, the filters [were] are baked at 350 °C for 60min. in an nitrogen atmosphere. Subsequently, a transparent polyimide layer [was] is formed as a leveling layer 505 by spin coat method.

On the entire surface of the structure, an ITO film of 0.1 μm thickness [was] is formed by sputtering and [was] is patterned into a common electrode 506 by the use of a fifth photomask 415. This ITO film [was] is formed at room temperature to 150 °C and annealed at 200 to 300 °C in an oxygen or an atmosphere. Thus, the second substrate [was] is completed.

A polyimide precursor material [was] is printed on the above -described substrates by an off-set method and baked at 350 °C for 1 hour in an non-oxide atmosphere, [e.g.] (e.g., in [a nitrogen] nitrogen). Then the surface of the polyimide [was] is subjected to a known rubbing method, so as to provide a means for orienting liquid crystal molecules in a fixed direction in at least an initial stage.

A nematic liquid crystal composition [was] is interposed

between the first and second substrates and the periphery of the substrates [was], is sealed with an epoxy adhesive. An drive IC in TAB form and a PCB comprising a common signal wiring and an electric potential wiring [were] are connected to the lead on the substrate, and a polarizing plate [was] is affixed to the outside, whereby a light-transmission type liquid crystal electro-optical device [was] is obtained.

Fig.24 shows the schematic configuration of the electro-optical device obtained in accordance with this embodiment. [ ]The liquid crystal panel 1000 obtained by the above steps [was] is combined with a back light device 1001 comprising three cool cathode tubes. Then a tuner 1002 for receiving TV electric waves [was] is connected thereto, to [thereby] complete an electro-optical device. Since the electro-optical device [thus] obtained [had] has a flat form compared with the conventional CRT type electro-optical device, it [was] is possible to hang it on the wall and the like.

[Next, the configuration of a peripheral circuitry of the liquid crystal electro-optical device is described with reference to Fig.25.]Next, the configuration of a peripheral circuitry of the liquid crystal electro-optical device is described with reference to Fig.25. The peripheral circuitry comprises a driver circuit 1103 connected to information signal side wires 1101 and 1102 which are connected to the matrix circuit of the liquid crystal electro-optical device. The driver circuit 1103 is divided into two drive frequency systems. One of them is a data latch circuit system 1104 having a drive method same as the conventional method, where the main composition is a basic clock CLK1[,] 1106 for transferring data 1105 by turns and 1-12 bits parallel processing [is conducted]. The other is the system composed in accordance with the present invention[, that is, it].

It is composed of a flip flop circuit 1108, a counter 1109 and a clock CLK2, 1107 for the independent frequency from the data transfer frequency. Pulses are formed by the counter 1109 so as to correspond to the gradated display data transmitted from the data latch system 1104.

[It is exactly this system which the] The present invention is [characterized by] directed to this type of system. That is, by utilizing two kinds of drive frequency, a clear digital gradated display can be obtained without reducing frame numbers for rewriting a picture. Accordingly, occurrence of flicker and the like due to the reduction of the frame number can be avoided.

On the other hand, in a driver circuit 1112 connected to scanning signal lines 1110 and 1111, the electric potential transmitted from a voltage level 1113 is controlled by a flip flop circuit 1115 of a clock CLK 1114 to supply address signals.

In the TFT obtained in accordance with this embodiment the mobility [was] is $80cm^2/Vs$, so that drive frequency [could] can be increased up to about 1 MHz. Therefore, a gradated display of up to 42 gradations [was] is possible, the gradation number being calculated by the following formula:

$$1\ MHz/(400*60)=42,$$

where 1 MHz represents the drive frequency, 400 the duty number, and 60 the frame number.

In the case of an [analogue] analog gradated display method, a gradated display of 16 gradations [was] is its limit due to the variation of the TFT characteristics. In the case of the digital gradated display method of the present invention, however, since the influence from the variation of the TFT characteristics is very little, a gradated display of 42 gradations is possible. In the case of a color display, a colorful, fine display of 74,088

colors is possible.

[[Embodiment 8]

This] The eighth embodiment of the present invention describes the manufacture of a video camera viewfinder utilizing a liquid crystal electro-optical device of 1 inch diagonal.

In this embodiment, a device utilizing amorphous TFTs in a 387x128 matrix by low temperature processing [was] is formed for a viewfinder. The manufacturing method of the liquid crystal display device utilized in this embodiment is explained below with reference to Fig.26.

A silicon oxide film of 1000 to 3000 Å thickness [was] is formed as a blocking layer 1201 on inexpensive glass 1200 such as soda-lime glass by magnetron RF (high frequency) sputtering method. The process conditions [were] are as follows:

Atmosphere: 100% oxygen;

Film Formation Temperature: 15 °C;

Output Power: 400-800W; and

Pressure: 0.5 Pa.

Quartz or single-crystal silicon [was] is utilized as a target, and the film formation speed [was] is 30 to 100 Å/min.

Then, a silicon film containing a 1 to 5 x $10^{21}cm^{-3}$ concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film [was] is formed, which [was] is then patterned with a first photomask 21 to form a gate electrode 1202 as in Fig.26(A). In this embodiment, the channel length [was] is 10um and as a gate electrode a phosphorus doped silicon film of

0.2 μm thickness [was] is formed and a molybdenum film of 0.3 μm thickness [was] is formed further thereon.

In the case of utilizing aluminum (Al) for the gate electrode material, after patterning with the first photomask 21 , it is possible to prevent the occurrence of cracks, voids in a channel region or an insulating layer on the gate electrode by anodic oxidation of this surface of the patterned aluminum gate electrode. Therefore, the TFT characteristics can be further increased by improving mobility and decreasing the threshold voltage.

A silicon oxide film [was] is then formed as a gate insulating film 1203 in the thickness range of 500 to 2000 Å[, e.g.] (e.g., 1000 Å[.]). This [was] is prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ions during the film formation.

An amorphous silicon film [was] is then formed on this structure by plasma CVD method. When forming a silicon film by plasma CVD, the temperature [was] is maintained at e.g. 300 °C and monosilane (SiH_4) or disilane (Si_2H_6) [was] is utilized. The gas [was] is introduced into a PCVD apparatus and a high frequency electric power of 13.56MHz [was inputted] is input thereto, whereby the film [was] is formed.

With respect to the film formed by the above method, it is preferable that the oxygen concentration is $5x10^{21}cm^{-3}$ or less. If the oxygen concentration is higher than this range, the mobility is decreased. If the concentration is too low, the current leak in the OFF state increases because of the back light. For this reason, the concentration is held in the range from $4x10^{19}$ to $4x10^{21}cm^{-3}$. Silicon concentration [was] is assumed to be $4x10^{22}cm^{-3}$.

Hydrogen concentration [was] is $4x10^{20}cm^{-3}$ which is equal to one atomic % of the silicon concentration. In accordance with the above method, a silicon film in an amorphous state [was] is formed to be 500 to 5000 Å[, e.g. 1500 Å] thick (e.g., 1500 Å).

Then, a resist film 1204 for forming a contact region by lift-off method [was] is formed utilizing a second photomask 22 , and on the top surface a silicon film 1205 to be an n-type activation layer [was] is formed by plasma CVD. The film formation temperature [was] is in the range from 250 °C to 350 °C [;] (at 320 °C in [this embodiment] the present embodiment). Monosilane and monosilane-based phosphine (PH_3) at a concentration of 1% and hydrogen (H_2) [were] are introduced at a ratio of 5 : 3 : 20 into a PCVD apparatus at a pressure of 5 Pa and a high frequency electric field at 13.56MHz [was] is applied to form the silicon film. At this moment, a high frequency electric power of 0.05 to $0.20W/cm^2$ [was] is appropriate, and an electric power of $0.120W/cm^2$ [was] is utilized in this embodiment.

The [thus] formed silicon film 1205 to be an n-type activation layer [had] has a specific electric conductivity of about 2×10^{-1} ncm^{-1}. The film thickness thereof [was] is 50 Å. Then, aluminum film 1206 of 3000 Å thickness [was] is formed for a lead and a contact electrode by sputtering. Unnecessary portions of the aluminum film [were] are removed by lift-off method to form a source region 1207 and a drain region 1208.

After forming each TFT 1209 in the form of island by the use of a third photomask 23 , an organic resin 1210 for surface flattering[, e.g.] (e.g., a transparent polyimide resin[, was]), is applied as shown in Fig.12(D), and an opening for electrode [was] is again formed by the use of a photomask 24 .

In order to connect the output end of the NTFT to one of transparent pixel electrodes of the liquid crystal device, an ITO (Indium Tin Oxide) film [was] is formed by sputtering method. The ITO film [was] is subjected to etching by using a photomask 25 to form an electrode 1211. The ITO film [was] is formed at room temperature to 150 °C and annealed at 200 °C to 400 °C in an oxygen or an atmosphere. Thus, an NTFT 1209 and an electrode 1211 made of a transparent conductive film [were] are formed on an identical glass substrate 1200. The electrical characteristics of the thus obtained TFT [were] are as follows:

Mobility: 0.2cm^2/Vs; and

Vth: 5.3V.

Next, in the same manner as [in Embodiment 7] described with respect to the seventh Embodiment of the present invention, color filters and a transparent conductive film of ITO [were] are formed to a thickness of 1000 Å on an insulating substrate to obtain a second substrate.

On the substrates, a polyimide precursor material [was] is printed by off-set printing and baked at 350 °C for 1 hour in an non-oxidation atmosphere[, e.g.] (e.g., in nitrogen). The surfaces of the polyimide [were] are then subjected to a known rubbing treatment [so as] to provide a means for orienting liquid crystal molecules in a fixed direction in at least an initial stage. Thus, the first and second substrates [were] are completed.

Then a nematic liquid crystal composition [was] is interposed between the first and the second substrates, and the periphery thereof [was] is sealed with an epoxy adhesive. Since the pitch of the leads on the substrate [was] is so fine as 46 μm, the connection [was] is carried out by the use of COG method. In this

embodiment, leads [were] are connected to gold bumps provided on an IC chip by means of a silver paradium resin of epoxy system[, and then]. Then an epoxy transformed acrylic resin [was] is filled in the space between the substrate and the IC chip for the purpose of fixing and enclosing the IC chip and the substrates. Then a polarizing plate [was] is affixed to the outside thereof, whereby a light-transmission type liquid crystal display device [was] is obtained.

With the TFT prepared in accordance with [this] the present embodiment, the mobility of $0.2cm^2/Vs$ [could] can be obtained in spite of the amorphous state, and accordingly the drive frequency [could] can be increased to about 100KHz. Therefore, a gradated display having 13 gradations [was] is possible, the gradation number being calculated by the following formula:

100 KHz / (128 * 60) = [13where] 13,

where 100KHz represents a drive frequency, 128 duty number, and 60 a frame number.

When carrying out the usual [analogue] analog gradated display with a liquid crystal electro-optical device of 50mm square size (the substrate of which size is obtained by dividing 300mm square substrate into 36 plates) on which TFTs of 384 x 128 = 49,152 [were] are formed, the variation of the amorphous TFT characteristic [was] is about ±10%, so that a gradated display of 8 gradations [was] is its limit. In the case of carrying out the digital gradated display method of the present invention, the method [was] is not affected by the variation of TFT characteristic so much, so that a gradated display of 13 gradations or more [was] is possible. In the case of a color display, a colorful, fine display of 2027 colors [was] is possible.

[[Embodiment 9]

This] The ninth embodiment [describes] of the present invention the manufacture of a projection type image display device as shown in Fig.27 is described. In this embodiment of the invention, an image projecting part for a projection type image display device [was] is assembled using three liquid crystal electro-optical devices 1300. Each of them [had] has a 640x480 dot matrix, and 307,200 pixels [were] are formed within the size of 4 inch diagonal. The size of one pixel [was] is 127 μm square.

The projection type image display device is composed of three liquid crystal electro-optical devices 1300 for three primary colors of light[, i.e.] (i.e., red, green, and blue respectively), a red color filter 1301, a green color filter 1302, a blue color filter 1303, reflection boards 1304, a metal halide light source 1307 of 150W, and an optical system for focus 1308.

The substrate of the liquid crystal electro-optical device utilized for an electro-optical device of this embodiment [was the one having the] has an NMOS configuration and a matrix circuitry. A device comprising high mobility TFTs formed by low temperature process [was] is utilized to compose the projection type liquid crystal electro-optical device.

The manufacturing method for the liquid crystal display device utilized in this embodiment is explained hereinafter with reference to Fig.28. A silicon oxide film of 1000 to 3000 Å thickness [was] is formed as a blocking layer 1401 on glass 1400 by magnetron RF (high frequency) sputtering as shown in Fig.28(A). The glass [was] is the one which [was] is not expensive unlike quartz glass [or so and was] and the like, and is resistant to thermal treatment at a temperature not higher

than 700 °C[, e.g.] (e.g., about 600 °C). The process conditions of the film formation [were] are the same as those for the silicon oxide film as a blocking layer in [Embodiment 1] the first embodiment of the invention.

On the silicon oxide film, a silicon film in an amorphous state [was] is formed to be 500 to 5000 Å thick, e.g. 1500 Å thick, in the same manner as the case of the silicon film in an amorphous state in [Embodiment 1] the first embodiment of the invention.

As in [Embodiment 1] the first embodiment, the silicon film in an amorphous state [was] is then annealed at an intermediate temperature of 450 °C to 700 °C for 12 to 70 hours in a non-oxide atmosphere.

Then the silicon film [was] is subjected to photo etching by the use of a first photomask 31 to form a region 1402 for TFT (having a channel width of 20 μm), as shown in Fig.28(A). [ ]A silicon oxide film of 500 to 2000 Å in thickness[, e.g.] (e.g., 1000 Å [thickness, was then]) is formed as a gate insulating film 1403. The formation conditions [thereof were] are the same as those for the silicon oxide film as a blocking layer. A small amount of fluorine may be added during the film formation for fixation of sodium ions.

Then, a silicon film containing a 1 to $5x10^{21}cm^{-3}$ concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film [was] is formed, which [was] is subsequently patterned with a second photomask 32 to form a gate electrode 1404 as in Fig.28(B). In this embodiment, a channel length [was] is made 10 μm, and as a gate electrode the phosphorus doped silicon of 0.2 μm thickness [was] is formed and

further a molybdenum film of 0.3 μm thickness [was] is laminated thereon. In Fig.28(C), phosphorus [was] is added by ion implantation method at a dosage of 1 to $5x10^{15}cm^{-2}$ to form a source 1405 and a drain 1406.

In the case of utilizing aluminum (Al) as a gate electrode material, after patterning with the second photomask 32 , it is possible to form the source and drain contact holes at positions closer to the gate by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

Next, heat annealing [was] is again carried out at 600 °C for 10 to 50 hours. Impurities in the source 1405 and the drain 1406 [were] are activated to make the source and drain N^+ regions. A channel forming region 1407 of semi-amorphous semiconductor [was] is formed below the gate electrode 1404.

The entire manufacturing process for the NTFT can thus be done without having to apply a temperature above 700 °C in spite of the self-aligning system. This makes it possible to use materials other than expensive ones such as quartz for substrates. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large number of pixels.

In this embodiment, the heat annealing process [was] is carried out twice as shown in Figs.28(A) and (C). However, the anneal process of Fig.28(A) may be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig.28(C), shortening the manufacturing time. In Fig.28(D), an interlayer insulating layer 1408 [was] is made of silicon oxide film using the sputtering method mentioned above.

This silicon oxide film can, however, be formed using [the] a LPCVD method, a photo CVD method or a normal pressure CVD method. The thickness of the insulating layer [was] is e.g. 0.2 to 0.6 μm.

Next, using photomask 33 , an opening 1409 for the electrodes [was] is formed. Then, a layer of aluminum [was] is formed over the entire structure using the sputtering method, and a lead 1410 and a contact 1411 [were] are formed using photomask 34.

An organic resin film 1412 for surface-flattering[, e.g.] (e.g., a transparent polyimide resin film [was]) is formed, and an opening for an electrode [was] is formed using photomask 35.

In order to connect the output terminal of the NTFT to the transparent electrode of the pixel of the liquid crystal device, an ITO (Indium Tin Oxide) film [was] is formed by sputtering. The ITO film [was] is etched by the use of a photomask 36 to form an electrode 1413. The ITO film [was] is formed at room temperature to 150 °C and annealed at 200 to 400 °C in an oxygen or an atmosphere.

Thus, the NTFT 1402 and the electrode 1413 of a transparent conductive film [were] are formed on an identical glass substrate 1400. The electrical characteristics of the obtained TFT [were] are as follows:

Mobility: 120cm^2/Vs; and

Vth: 5.0V.

A schematic view of the structure is shown in Fig.29. On the substrate (1500 in Fig.29) mentioned above, a mixture of 10um thickness [was] is formed by die-cast method, the mixture comprising fumaric acid polymeric resin and nematic liquid crystal both dissolved at a ratio of 65 : 35 in a common solvent, xylene. Then the above structure [was] is heated at 120 °C

for 180min. in a nitrogen atmosphere to remove the solvent, whereby a liquid crystal dispersion layer 1501 [was] is formed. It [was] is found that tact-time could be shortened by making the pressure a bit lower than the atmospheric pressure at the moment.

Then, an ITO film [was] is formed by sputtering to obtain an opposed electrode 1502. This ITO film [was] is formed at room temperature to 150 °C. A transparent silicon resin [was] is then applied to be 30um thick by printing method and [was] is baked at 100 °C for 30 min. to [thereby] obtain a liquid crystal electro-optical device.

The configuration and the function of the driver IC utilized in this embodiment is the same as that in [Embodiment 7] the seventh embodiment of the present invention.

When a usual [analogue] analog gradated display [was] is carried out with a liquid crystal electro-optical device where 307,200 TFTs in 640x480 dot matrix [were] are formed within 300mm square, the variation in TFT characteristics [was] is as large as about ±10%, so that a gradated display of up to 16 gradations [was] is its limit. In the case of the TFTs formed in this embodiment, however, since the drive frequency can be increased up to 2.5MHz, a gradated display of up to 86 gradations is possible, the gradation number being calculated by the following formula:

$$2.5\text{MHz}/(480\text{x}60)=86$$

where 2.5MHz represents the drive frequency, 480 the number of scanning lines, and 60 the number of frames.

In the case of the digital gradated display method in accordance with this embodiment, the method is not affected by the variation in TFT characteristics [so] much, so that a gradated display of 86 gradations is possible. With regard to a

color display, a colorful, fine display having 262,144 colors can be obtained.

A conventional television set utilizing a liquid crystal display having 16 gradations is not suitable for displaying a natural landscape[, for]. For example, a hollow (uneven) surface of a 'lock' of one color[, since a hollow (uneven) surface of the 'lock' of one color] should be displayed by subtly different colors in order to express a variety of shades of the hollow (uneven) surface in sunshine. However, the gradated display, in accordance with the present invention, makes it possible to project a picture[, e.g.] (e.g., a 'lock' of one color[,]) with variations of fine tone.

This liquid crystal electro-optical device is applicable not only to a front type projection TV as shown in Fig.27 but also a rear type projection TV.

[[Embodiment 10]

This] The tenth embodiment of the present invention shows the manufacture of an electro-optical device for a portable computer utilizing a liquid crystal dispersion type display device of reflection type as shown in Fig.30.

The first substrate utilized in this embodiment [was] is formed by the same steps as in [Embodiment 7] the seventh embodiment of the invention.

This embodiment will be explained below utilizing the liquid crystal electro-optical device shown in [Fig.29] Fig. 29. Fumaric acid polymeric resin and a nematic liquid crystal mixed with a black pigment at 15% [were] are dissolved in a common

solvent, xylene at a ratio of 65 : 35. This solution [was] is formed to a thickness of 10um on the substrate 1500 by die-cast method and [was] is then heated at 120 °C for 180 min. in a nitrogen atmosphere to remove the solvent, whereby a liquid crystal dispersion layer 1501 [was] is obtained.

Then, an ITO film [was] is formed by sputtering to obtain an opposed electrode 1502. This ITO film [was] is formed at room temperature to 150 °C. Then, a silicon resin of white color of 55um thickness [was] is applied on the rear surface by printing method and baked at 100 °C for [90min] 90 minutes to obtain a liquid crystal electro-optical device.

By utilizing the black pigment as the above, it became possible to display black color displayed when the light [was] is dispersed (i.e. when no electric fields [were] are applied) and also white color when the light [was] is transmitted (i.e. when electric fields [were] are applied), whereby a display as if characters [were] are written on a paper could be obtained.

Alternatively, it [was] is possible to display white color when the light [was] is dispersed and black color when the light [was] is transmitted, without mixing the black pigment. In this case, however, it [was] is necessary to make the rear surface black. A display as if characters [were] are written on a paper could be also obtained.

[[Embodiment 11]

This] The eleventh embodiment of the present invention shows the manufacture of a television set to be hanged on the wall utilizing a liquid crystal display device having the circuit configuration shown in Fig.31. TFTs utilized therein are made of polycrystalline silicon subjected to laser annealing and in

stagger type.

Fig. 32 shows the layout of the actual electrodes and the like corresponding to the circuit configuration in Fig.31. [ ]In order to simplify the explanation, the parts corresponding to a 2x2 (or less) matrix only are shown therein. Also, the actual driving signal waveform is shown in Fig. 16. For simplicity, the explanation of the signal waveform is also given for the case of 2x2 matrix configuration.

The manufacturing process for a liquid crystal panel utilized in this embodiment is explained with reference to Fig.33.

In Fig.33(A), a silicon oxide film for a blocking layer 651 having a thickness of 1000 to 3000 Å [was] is formed on a glass substrate 650, using a magnetron RF (high frequency) sputtering method. The glass substrate 650 [was] is made of inexpensive materials glass capable of withstanding heat treatment up to 700 °C, e.g. about 600 °C.

The process conditions [were] are the same as those for the silicon oxide film as a blocking layer in [Embodiment 7] the seventh embodiment of the present invention. On the blocking layer 651, a silicon film 652 in an amorphous state [was] is formed to be 500 to 5000 Å thick, e.g. 1000 Å thick, in the same manner as that for the silicon film in an amorphous state in [Embodiment 7] described with respect to the seventh embodiment.

As shown in Fig.33(B), a photoresist pattern 653 with source and drain regions opened [was] is formed using a mask P1 . Then, a silicon film to be an n-type activation layer [was] is formed thereon by plasma CVD method. The film formation temperature [was] is maintained at 250 °C to 350 °C, specifically 320 °C in this embodiment. Monosilane (SiH_4) and monosilane-based phosphine (PH_3) at a concentration of 3% [were] are introduced into a PCVD

apparatus at a pressure of 5 Pa and a high frequency electric power at 13.56MHz [was] is inputted thereto, to thereby form the silicon film. A high frequency electric power of 0.05 to 0.20W/cm^2 [was] is appropriate, and a high frequency electric power of 0.120W/cm^2 [was] is inputted in this embodiment. The specific electric conductivity of the n-type silicon film thus obtained [was] is about $2x10^{-1}\Omega cm^{-1}$. The film thickness [was] is 50 Å.

On the other hand, a photoresist pattern 654 with source and drain regions opened [was] is formed using a mask P2 , as shown in Fig.33(C). Then, a silicon film to be a p-type activation layer [was] is formed thereon by plasma CVD method. The film formation temperature [was] is maintained at 250 °C to 350 °C, specifically 320 °C in this embodiment. Monosilane (SiH_4) and monosilane-based diborane (B_2H_6) at a concentration of 2% [were] are introduced into a PCVD apparatus at a pressure of 4 Pa and a high frequency electric power at 13.56MHz [was] is inputted to thereby form the silicon film. A high frequency electric power of 0.05 to 0.20W/cm^2 [was] is appropriate, and a high frequency electric power of 0.080W/cm^2 [was] is inputted in this embodiment. The specific electric conductivity of the p-type silicon film [thus] obtained [was] is about $1x\ 10^{-1}\ \Omega cm^{-1}$. The film thickness [was] is 50 Å.

Then, source and drain regions 655, 656 and 657, 658 [were] are formed by lift-off method. After that, an island region 663 for an N-channel type thin film transistor and an island region 664 for a P-channel type thin film transistor [were] are formed using a mask P3 662.

Subsequently, laser annealing to the source, drain, channel regions and laser doping to the activation layers [were] are carried out simultaneously by the use of XeCl excimer laser in

the same way as in [Embodiment 7] the seventh embodiment of the invention. An electron mobility (ue) of 15 to 300cm^2/Vsec and a hole mobility (ue) of 5 to 100cm^2/Vsec can be obtained.

A silicon oxide film of 500 to 2000 Å thickness, e.g. 1000 Å thickness, [was] is then formed as a gate insulating film. This [was] is prepared under the same conditions as the silicon oxide film formed as a blocking layer. A small amount of fluorine may be added to this film for fixation of the sodium ions during film formation.

When this operation [was] is completed, a silicon film containing phosphorus at 1 to $5x10^{21}cm^{-3}$ concentration, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2film [was] is formed[, which was]. The silicon film is patterned with a fourth photomask 669 to obtain the configuration shown in FIG. 33(E). Gate electrodes 666 and 667 [were] are then formed. For example, for gate electrodes a phosphorus-doped silicon layer 0.2 μm thick [was] is formed and a molybdenum layer 0.3 μm thick [was] is formed thereon with a channel length of 7 μm.

Also, in the case where aluminum is used as the gate electrode material, after patterning with the fourth photomask 669, it is possible to form the source and drain contact holes at positions closer to the gates by anodic oxidation of this surface of the patterned aluminum gate electrode so that self-aligning construction can be applied. Therefore, the TFT characteristics can be further increased by improving the mobility and decreasing the threshold voltage.

The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above 400 °C. This makes it possible to use, as the substrate, materials other than

expensive materials, such as quartz. Accordingly, this embodiment of the invention is very suitable for a liquid crystal display having a large picture plane.

In Fig.33(F), a silicon oxide film [was] is formed as an interlayer insulator 668 by a sputtering method. In place of the sputtering method, LPCVD method, photo CVD method, and normal pressure CVD may be utilized for the formation of the silicon oxide film. The thickness of the layer [was] is 0.2 to 0.6um, for example. After that, an opening 679 for electrode [was] is formed using a fifth photomask 670. On the entire surface of this structure, an aluminum film having a thickness of 0.3 μm [was] is formed by sputtering method, and then a lead 674 and a contact 673 [were] are formed using a sixth photomask 676.

A silicon oxide film [was] is again formed as an interlayer insulating layer 680 by the above mentioned sputtering method. Instead of the sputtering method, the LPCVD method, the photo CVD method, and the normal pressure CVD method [may] can also be utilized for forming the silicon oxide film. The silicon oxide film [was] is then patterned using a seventh photomask 681. Then, on the entire surface an aluminum film of 0.3 μm thickness [was] is formed by sputtering. A lead 683 and a contact 684 [were] are then formed using an eighth photomask 682.

An organic resin for surface-flattering 685[, e.g.] (e.g., a transparent polyimide resin [was then]) is applied on the top surface, and further an opening for electrode [was] is again formed using a ninth photomask 686.

An ITO film of 0.1 μm thickness [was] is formed on the entire surface of this structure by sputtering and [was] is subsequently patterned into pixel electrodes 688 by the use of a tenth photomask 687. This ITO film [was] is formed at room temperature to 150 °C and annealed at 200 °C to 400 °C in an oxygen or an

atmosphere.

The electrical characteristics of the thus formed NTFT and PTFT [were] are as follows:

NTFT ... Mobility: $80cm^2/Vs$,

Vth: 5.0V; and

PTFT ... Mobility: $30cm^2/Vs$,

Vth: 5.5V.

In accordance with the foregoing method, the first substrate for a liquid crystal electro-optical device [was] is completed.

A second substrate for the liquid crystal electro-optical device [was] is formed in the same manner as in [Embodiment 7] the seventh embodiment of the invention.

A nematic liquid crystal composition [was] is interposed between the first and second substrates and the periphery of the substrates [was] is sealed with an epoxy adhesive. [An] A driver IC in TAB form and a PCB comprising a common signal wiring and a potential wiring [were] are connected to the lead on the substrate, and a polarizing plate [was] is affixed to the outside whereby a light-transmission type liquid crystal electro-optical device [was] is obtained.

The structure of the electro-optical device obtained in accordance with this embodiment is the same as that in [Embodiment 7] the seventh embodiment of the invention and schematically illustrated in Fig.24.

Next, the configuration of a peripheral circuitry of the liquid crystal electro-optical device is described with reference to Fig.34.

A driver circuit 352 is connected to information signal side

wires 350 and 351 which are connected to the matrix circuit of the liquid crystal electro-optical device. The driver circuit 352 is divided into two drive frequency systems. One of them is a data latch circuit system 353 having a [drive method same as the] conventional drive method, where the main composition is a basic clock OH 355 for transferring data 356 by turns and 1-12 bits parallel processing is conducted. The other frequency drive system is the system composed in accordance with the present invention[, that]. That is, [it] the system is composed of a magnitude comparator circuit 358, a buffer 360 for panel drive and a clock CLK 357 for the independent [frequency] determination of the data transfer frequency. Pulses are formed by the counter 358 so as to correspond to the gradated display data transmitted from the data latch system 353.

[It is exactly this system which the] The present invention is [characterized by] directed to this system. That is, by utilizing two kinds of drive frequency, a clear digital gradated display can be obtained without reducing frame numbers for rewriting a picture. Accordingly, occurrence of flicker, and the like, due to the reduction of the frame number can be avoided.

Fig.35 is a photograph of oscilloscope showing input signal waveforms [inputted] input to and output signal waveforms [outputted] output from the C/TFT obtained in this embodiment. In Figs.35(A) to (D), the drive frequency of input signals is raised as 5KHz, 50KHz, 500KHz, and 1MHz. As is apparent from Fig.35(D), even at 1MHz, output signal waveforms do not become gentle so much and fully useful output signals can be obtained.

The number of gradations of a gradated display can be calculated by dividing the drive frequency by duty number and frame number. In the case of the drive frequency of 1MHz, a gradated display of 42 gradations (calculated by dividing 1MHz by

400 and 60) can be obtained.

In [the case of an analogue] an analog gradated display method, a gradated display of 16 gradations [was] is its limit due to the variations in TFT characteristics. In the case of the digital gradated display method of the present invention, however, since the method is not affected by the variations in TFT characteristics so much, a gradated display of up to 42 gradations is possible. With regard to a color display, a colorful, fine display of 74,088 colors can be obtained.

[[Embodiment 12]

This] The twelfth embodiment of the present invention shows the manufacture of a video camera viewfinder utilizing a liquid crystal electro-optical device of 1 inch diagonal.

In this embodiment, a first substrate with 387x128 pixel configuration [was] is prepared by the same process as in [Embodiment 11] the eleventh embodiment described above. Also,a second substrate [was] is prepared by providing color filters and a transparent conductive film ITO to a thickness of 1000 Å on a substrate made of insulator by the same process as in [Embodiment 11] the eleventh embodiment described above.

On the above substrates, a polyimide precursor material [was] is printed by off-set method, and subsequently the substrates [were] are baked at 350 °C for 1 hour in an non-oxidizing atmosphere[, e.g.] (e.g., in [a nitrogen] nitrogen). Then, the surfaces of the polyimide films [were] are subjected to a [know] known rubbing treatment, whereby the first and second substrate provided with means for orientating liquid crystal molecules in one fixed direction in at least an initial stage [were] are obtained.

A nematic liquid crystal composition [was] is interposed between the above first and second substrates and the periphery of the substrates [was] is sealed with an epoxy adhesive. Since the pitch of the leads on the substrates [was] is as fine as 46 μm, connection [was] is conducted by COG method. In this embodiment, leads [were] are connected to gold bumps provided on an IC chip by means of a silver paradium resin of epoxy system, and then an epoxy transformed acrylic resin [was] is filled in the space between the IC chip and the substrates for the purpose of fixing and enclosing the IC chip. Then a polarizing plate [was] is affixed to the outside thereof, whereby a light-transmission type liquid crystal display device [was] is obtained.

Since the channel length [was] is 5 μm in the TFT of this embodiment, the drive frequency [could] can be raised up to about 2MHz. Hence, in accordance with the division of 2MHz by 128 and 60, 260 gradations, approximately 256 gradations [were] are possible in a gradated display. When carrying out the usual [analogue] analog gradated display with a liquid crystal electro-optical device of 50mm square size (the substrate of which size is obtained by dividing 300mm square-sized substrate into 36 plates) on which TFTs of 384x128 = 49,152 [were] are formed, the variation in the amorphous TFT characteristic [was] is about ±10%, so that a gradated display of 16 gradations [was] is its limit. In the case of carrying out the digital gradated display method of the present invention, the method [was] is not affected by the variation in TFT characteristic so much, so that a gradated display of 256 gradations or more [was] is possible. In the case of a color display, a colorful, fine display of 16,777,216 colors [was] is possible.

[[Embodiment 13]

This] The thirteenth embodiment of the invention describes the manufacture of a projection type image display device as shown in Fig.27. In this embodiment, an image projecting part for a projection type image display device [was] is assembled using three liquid crystal electro-optical devices 1300. Each of them [had] has a 640x480 dot matrix, and 307,200 pixels [were] are formed within the size of 4 inch diagonal. The size of one pixel [was] is 127 μm square.

The projection type image display device is composed of three liquid crystal electro-optical devices 1300 for three primary colors of light[, i.e.] (i.e., red, green, and blue respectively), a red color filter 1301, a green color filter 1302, a blue color filter 1303, reflection boards 1304, a metal halide light source 1307 of 150W, and an optical system for focus 1308.

The substrate of the liquid crystal electro-optical device utilized for an electro-optical device of this embodiment [was] is the one having C/TFT configuration and a matrix circuitry. A device comprising high mobility TFTs formed by low temperature process [was] is utilized to compose the projection type liquid crystal electro-optical device.

The manufacturing method for the liquid crystal display device utilized in this embodiment is explained hereinbelow with reference to [Fig.36] Figs. 36(A)-36(G). In Fig.36(A), a silicon oxide film of 1000 to 3000 Å thickness [was] is formed as a blocking layer 602 on glass 601 by a magnetron RF (high frequency) sputtering. The glass [was] is the one which [was] is not expensive unlike quartz glass [or so and was] and the like, and is resistant to thermal treatment at not higher than 700 °C[, e.g.] (e.g., about 600 °C). The process conditions of the film formation [were] are the same as those for the silicon oxide film as a blocking layer in [Embodiment 1] the first embodiment of the

invention.

On the silicon oxide film, a silicon film 603 in an amorphous state [was] is formed to be 500 to 5000 Å thick, e.g. 1500 Å thick, in the same manner as the case of the silicon film in an amorphous state in [Embodiment 1] the first embodiment of the invention.

As in [Embodiment 1] the first embodiment, the silicon film in an amorphous state [was] is then heat-annealed at an intermediate temperature of 450 °C to 700 °C for 12 to 70 hours in an non-oxide atmosphere.

A silicon oxide film 604 of 500 to 2000 Å thickness, e.g. 1000 Å thickness, [was] is then formed as a gate insulating film. The formation conditions thereof [were] are the same as those for the silicon oxide film as a blocking layer. A small amount of fluorine may be added during the film formation for fixation of sodium ions.

Then, a silicon film containing a 1 to $5x10^{21}cm^{-3}$ concentration of phosphorus, or a multilayered film comprising the silicon film laminated thereon with molybdenum (Mo), tungsten (W), $MoSi_2$ or WSi_2 film [was] is formed, which [was] is subsequently patterned with a first photomask 41 as in Fig.36(B). In this embodiment, a molybdenum film [was] is formed to a thickness of 0.3 μm as a gate electrode with a channel length of 10 μm. In the patterning, the gate electrodes [were] are overetched 77 at about 3 μm. Then, a positive photoresist 607 [was] is applied on the entire surface of the substrate.

After the application, exposure and development [were] are carried out from the rear side of the substrate, using a photomask 42 to thereby obtain a resist 608. Then, an n-type layer [was] is deposited by sputtering. By subsequently removing

the resist 608 by lift-off method, the configuration shown in Fig.36(D) [was] is obtained.

In the same manner, after a positive photoresist [was] is applied on the entire surface of the substrate, exposure and development [were] are carried out from the rear side of the substrate using a photomask 43 to thereby obtain a resist 610. Then a p-type layer [was] is deposited by sputtering. By removing the resist 610 by lift-off method, the configuration shown in Fig.36(E) [was] is obtained.

The substrate [was] is again heat-annealed at 600 °C for 10 to 50 hours, whereby impurities in sources 612, 614 and drains 613, 615 [were] are activated to be N^+ or P^+ type. Channel formation regions 618 and 619 of semi-amorphous semiconductor [was] is formed below gate electrodes 616 and 617. The entire manufacturing process for the C/TFT can thus be done without having to apply a temperature above 700 °C in the self-aligning system. This makes it possible to use materials other than expensive ones, such as quartz, as the substrate material. Accordingly, this embodiment of the invention is [very] suitable for a liquid crystal display having a large picture plane.

The heat anneal process, shown in fig.36(A) and Fig.36(E), [was] is performed twice. However, the anneal process in Fig.36(A) can be omitted, depending on the desired characteristics, and followed up with the heat anneal process of Fig.36(E), shortening the manufacturing time.

In Fig.36(F), a silicon oxide film [was] is formed as an interlayer insulator 620 by the sputtering method mentioned above. This silicon oxide film may be formed by the LPCVD method, photo CVD method, or normal pressure CVD method, instead. The thickness of the insulator [was] is, e.g., 0.2 to 0.6 μm. Next, using a photomask 44, openings 621 for the electrodes [were] are

formed. Then, a layer of aluminum [was] is formed on the entire structure using the sputtering method, and a lead 622 and a contact 623 [were] are formed using a photomask 45, as shown in Fig.36(F).

An organic resin film 624 for surface-flattering[, e.g.] (e.g., a transparent polyimide resin film [was]) is formed, and electrode an opening for an electrode [was] is provided using a photomask 46 .

In order to connect the output terminal of the C/TFT to the (transparent) electrode of the pixel of the liquid crystal display device, an ITO film [was] is formed by sputtering. [ ]The electrode 625 [was] is completed by etching through a photomask 47 .

This ITO film [was] is formed in the range from room temperature to 150 °C and annealed at 200 °C to 400 °C in oxygen or atmosphere. The NTFT 626, PTFT 627, and the transparent electrode 625 [were] are thus prepared on an identical glass substrate 601. The electrical characteristics of the TFTs thus obtained are as follows:

NTFT [%%%]... Mobility: 120cm^2/Vs,

Vth: 5.0V; and

PTFT [%%%]... Mobility: 50cm^2/Vs,

Vth: 5.3V.

The substrate 1500 shown in Fig.29 [was] is obtained by the foregoing process.

A liquid crystal dispersion layer 1501 [was] is formed on the substrate 1500 in the same manner as in [Embodiment 9] the ninth embodiment described above, as shown in Fig.29. Further an opposed electrode 1502 [was] is formed thereon as in [Embodiment

9] the ninth embodiment. Then, a transparent silicon resin of 30 μm thickness [was] is applied on the top surface of the structure by printing method and [was] is baked at 100 °C for 30 min. to thereby obtain a liquid crystal electro-optical device. [

]The configuration and the function of the driver IC utilized in this embodiment are the same as in [Embodiment 11] the eleventh embodiment.

When a usual [analogue] analog gradated display [was] is carried out with a liquid crystal electro-optical device where 307,200 TFTs in 640x480 dot matrix [were] are formed within 300mm square, the variation in TFT characteristics [was] is as large as about ±10%, so that a gradated display of up to 16 gradations [was] is its limit. In the case of the TFTs formed in this embodiment, however, since the drive frequency can be increased up to 2.5MHz, a gradated display of up to 86 gradations is possible, the gradation number being calculated by the following formula:

$$2.5\text{MHz}/(480\text{x}60)=86$$

where 2.5MHz represents the drive frequency, 480 the number of scanning lines, and 60 the number of frames. With regard to a color display, a colorful, fine display having 262,144 colors can be obtained. [

]This liquid crystal electro-optical device is applicable not only to a front type projection TV shown in Fig.27 but also to a rear type projection TV.

[[Embodiment 14]

This] The fourteenth embodiment of the present invention shows the manufacture of an electro-optical device for a portable

computer utilizing a liquid crystal dispersion type display device of reflection type as in Fig.30. A first substrate 1500 utilized in this embodiment [was] is formed in the same manner as in [Embodiment 11] the eleventh embodiment.

As shown in Fig.29, a liquid crystal dispersion layer 1501, a counter electrode 1502 on the layer 1501, and a transparent silicon resin on the electrode 1502 [were] are provided on the substrate 1500 as in [Embodiment 10] the tenth embodiment, described above. The silicon resin [was] is subsequently baked at 100 °C for 90 min. to thereby obtain a liquid crystal electro-optical device.

In the present invention, a gradated display is provided using a display drive system with the display timing related to the unit time t for writing-in a picture element and to the time F for writing-in one picture, wherein, by time-sharing the signal during a write-in of time t, without changing the time F, a clear gradated display controlled by digital can be obtained. Compared with the gradated display method using a plurality of frames, a display of high quality is possible without the decrease of display frequency by the digital gradated display method of the present invention.

Instead of a conventional [analogue] analog gradated display, the present invention provides a digital gradated display with two kinds of drive frequencies being independent of each other. In the case of utilizing a liquid crystal electro-optical device in 640x400 dot matrix, conventionally it was very difficult to form all the 256,000 TFTs without variations in characteristic, and taking the actual productivity and yields into consideration , a gradated display of 16 gradations [was] is its limit. On the other hand, in order to make clear the applied voltage level, a reference voltage value is inputted, instead of an [analogue]

analog value, as a signal from the controller side in the present invention. By controlling by a digital value the timing to connect the reference signal to TFT, the voltage applied to the TFT is controlled, whereby the variation in TFT characteristics is covered. Hence, a clear digital gradated display is possible in accordance with the present invention.

The use of two kinds of drive frequencies makes it possible to obtain a clear digital gradated display without changing the number of frames for rewriting a picture, [whereby] and the occurrence of flicker and the like, due to the decrease of the frame number, can be avoided.

ABSTRACT

An electro-optical device comprising a display drive system with the display timing related to the unit time t for writing-in a picture element and to the time F for writing-in one picture is disclosed. In the device, a gradated display corresponding to the ratio of the division can be obtained by time-sharing the signal during a write-in of time t without changing the time F.